TS64MLD64V5F

184PIN DDR500 Unbuffered DIMM
512MB With 32Mx8 CL3

Description

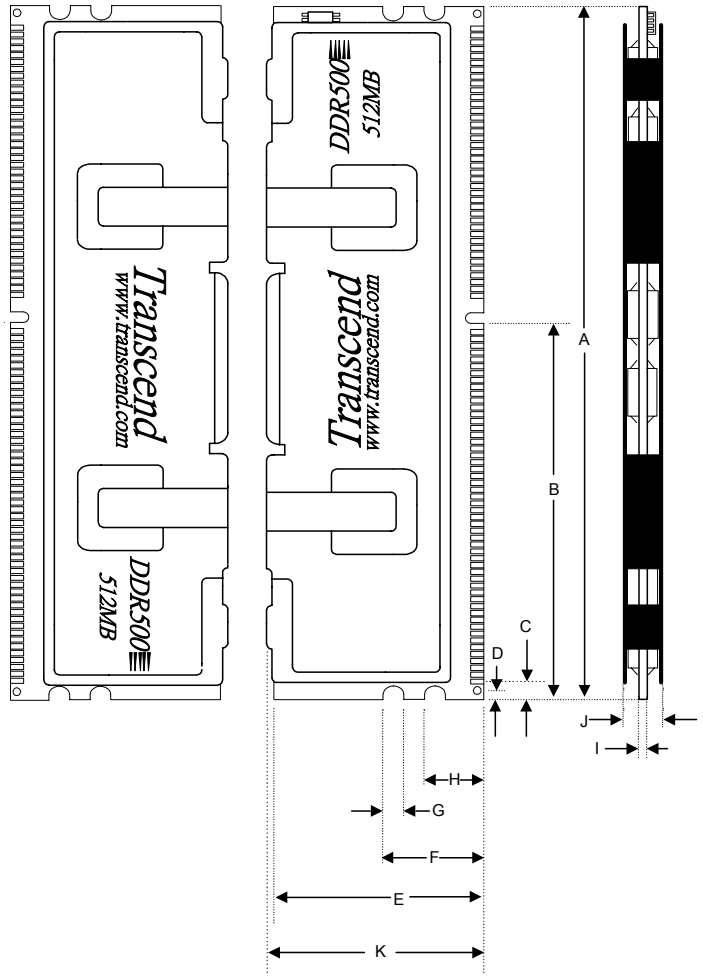
The TS64MLD64V5F is a 32M x 64bits Double Data Rate SDRAM high-density for DDR500.The TS64MLD64V5F consists of 16pcs CMOS 32Mx8 bits Double Data Rate SDRAMs in 66 pin TSOP-II 400mil packages and a 2048 bits serial EEPROM on a 184-pin printed circuit board. The TS64MLD64V5F is a Dual In-Line Memory Module and is intended for mounting into 184-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- Power supply: VDD: 2.6V ± 0.1V, VDDQ: 2.6V ± 0.1V
- Max clock Freq: 250MHZ.
- Double-data-rate architecture; two data transfers per clock cycle
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transition with CK transition
- Auto and Self Refresh 7.8us refresh interval.
- Data I/O transactions on both edge of data strobe.
- Edge aligned data output, center aligned data
- Serial Presence Detect (SPD) with serial EEPROM
- SSTL-2 compatible inputs and outputs.
- MRS cycle with address key programs.
  CAS Latency (Access from column address): 3
  Burst Length (2,4,8)
  Data Sequence (Sequential & Interleave)

Placement



PCB: 09-1860

Dimensions

Side	Millimeters	Inches
A	133.35±0.20	5.250±0.008
B	72.40	2.850
C	6.35	0.250
D	2.20	0.087
E	30.48±0.20	1.200±0.008
F	19.80	0.800
G	4.00	0.157
H	12.00	0.472
I	1.27±0.10	0.050±0.004
J	7.5(Max)	0.3(Max)
K	32.28±0.30	1.271±0.012

(Refer Placement)

Pin Identification

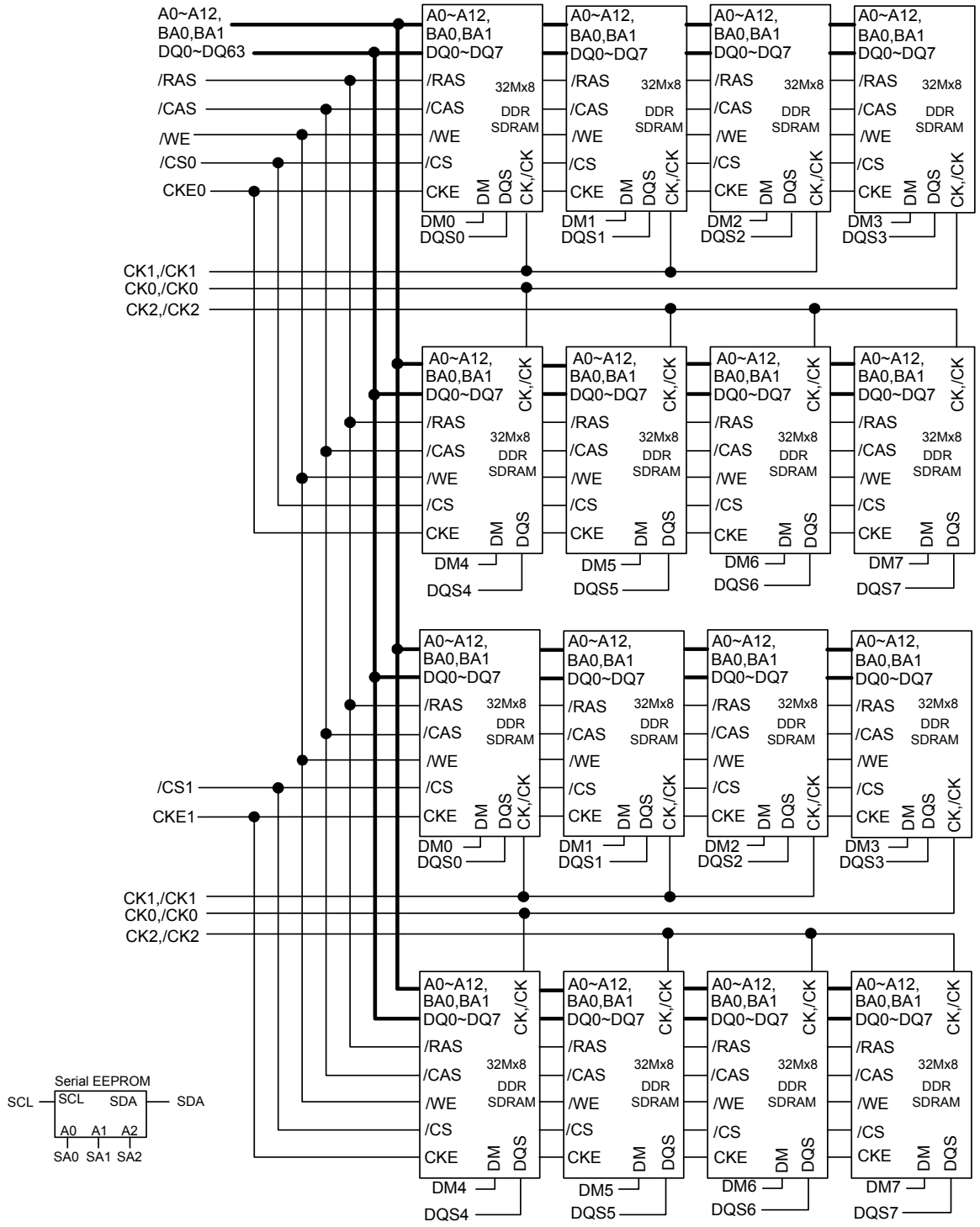
Symbol	Function
A0~A12, BA0, BA1	Address input
DQ0~DQ63	Data Input / Output.
DQS0~DQS7	Data strobe input/output
CK0, /CK0 CK1, /CK1 CK2, /CK2	Clock Input.
CKE0, CKE1	Clock Enable Input.
/CS0, /CS1	Chip Select Input.
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DM0~DM7	Data-in Mask
VDD	+2.5 Voltage power supply
VDDQ	+2.5 Voltage Power Supply for DQS
VREF	Power Supply for Reference
VDDSPD	+2.5 Voltage Serial EEPROM Power Supply
SA0~SA2	Address in EEPROM
SCL	Serial PD Clock
SDA	Serial PD Add/Data input/output
VSS	Ground
NC	No Connection

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREF	47	*DQS8	93	VSS	139	VSS
02	DQ0	48	A0	94	DQ4	140	*DM8
03	VSS	49	*CB2	95	DQ5	141	A10
04	DQ1	50	VSS	96	VDDQ	142	*CB6
05	DQS0	51	*CB3	97	DM0	143	VDDQ
06	DQ2	52	BA1	98	DQ6	144	*CB7
07	VDD	53	DQ32	99	DQ7	145	VSS
08	DQ3	54	VDDQ	100	VSS	146	DQ36
09	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	VDD
11	VSS	57	DQ34	103	NC	149	DM4
12	DQ8	58	VSS	104	VDDQ	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	VSS
15	VDDQ	61	DQ40	107	DM1	153	DQ44
16	*CK1	62	VDDQ	108	VDD	154	/RAS
17	*/CK1	63	/WE	109	DQ14	155	DQ45
18	VSS	64	DQ41	110	DQ15	156	VDDQ
19	DQ10	65	/CAS	111	*CKE1	157	/CS0
20	DQ11	66	VSS	112	VDDQ	158	*/CS1
21	CKE0	67	DQS5	113	NC	159	DM5
22	VDDQ	68	DQ42	114	DQ20	160	VSS
23	DQ16	69	DQ43	115	*A12	161	DQ46
24	DQ17	70	VDD	116	VSS	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	VSS	72	DQ48	118	A11	164	VDDQ
27	A9	73	DQ49	119	DM2	165	DQ52
28	DQ18	74	VSS	120	VDD	166	DQ53
29	A7	75	*/CK2	121	DQ22	167	NC
30	VDDQ	76	*CK2	122	A8	168	VDD
31	DQ19	77	VDDQ	123	DQ23	169	DM6
32	A5	78	DQS6	124	VSS	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	VSS	80	DQ51	126	DQ28	172	VDDQ
35	DQ25	81	VSS	127	DQ29	173	NC
36	DQS3	82	NC	128	VDDQ	174	DQ60
37	A4	83	DQ56	129	DM3	175	DQ61
38	VDD	84	DQ57	130	A3	176	VSS
39	DQ26	85	VDD	131	DQ30	177	DM7
40	DQ27	86	DQS7	132	VSS	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	VSS	88	DQ59	134	*CB4	180	VDDQ
43	A1	89	VSS	135	*CB5	181	SA0
44	*CB0	90	NC	136	VDDQ	182	SA1
45	*CB1	91	SDA	137	CK0	183	SA2
46	VDD	92	SCL	138	/CK0	184	VDDSPD

*Please refer Block Diagram

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on V_{DD} supply to Vss	VDD, VDDQ	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55~+150	°C
Power dissipation	P_D	24	W
Short circuit current	I_{OS}	50	mA
Mean time between failure	MTBF	50	year
Temperature Humidity Burning	THB	85°C/85%, Static Stress	°C-%
Temperature Cycling Test	TC	0°C ~ 125°C Cycling	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	VDD	2.5	2.7	V	
I/O Supply voltage	VDDQ	2.5	2.7	V	
I/O Reference voltage	VREF	V_{DDQ}/2-50mV	V_{DDQ}/2+50mV	V	1
I/O Termination voltage	VTT	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	VIH(DC)	V_{REF}+0.15	V_{DDQ}+0.3	V	4
Input logic low voltage	VIL(DC)	-0.3	V_{REF}-0.15	V	4
Input Voltage Level, CK and /CK inputs	VIN(DC)	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CK and /CK inputs	VID(DC)	0.3	V_{DDQ}+0.6	V	3
Input crossing point voltage, CK and /CK inputs	VIX(DC)	1.15	1.35	V	5
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current (Normal strength driver) VOUT= VTT + 0.84V	I_{OH}	-16.8		mA	
Output Low Current (Normal strength driver) VOUT= VTT – 0.84V	I_{OL}	16.8		mA	
Output High Current (Half strength driver) VOUT= VTT + 0.45V	I_{OH}	-9		mA	
Output High Current (Half strength driver) VOUT= VTT - 0.45V	I_{OL}	9		mA	

Note:
1. Includes ± 25mV margin for DC offset on VREF, and a combined total of ± 50mV margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled. TO VREF, both of which may result in VREF noise. VREF should be de-coupled with an inductance of <=3nH.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on /CK.
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 250MHZ.
5. The value of V_{IX} is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, V_{DD}=2.7V T_A = 10°C)

Parameter	Symbol	Max.	Unit	Note
Operating current - One bank Active-Precharge; tRC=tRCmin; DQ, DM and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle	IDD0	1,440	mA	
Operating current - One bank operation; One bank open, Burst=4; Reads refer to the following page for detailed test condition.	IDD1	1,640	mA	
Precharge power-down standby current; All banks idle; power-down mode; CKE = <VIL(max); VIN = VREF for DQ,DQS and DM	IDD2P	65	mA	
Precharge Floating standby current; CS# > =VIH(min);All banks idle; CKE > = VIH(min); Address and other control inputs changing once per clock cycle; VIN = VREF for DQ,DQS and DM	IDD2F	480	mA	
Active power - down standby current; one bank active; power-down mode; CKE<= VIL (max); VIN = VREF for DQ, DQS and DM	IDD3P	880	mA	
Active standby current; CS# >= VIH(min); CKE>=VIH(min); one bank active; active - precharge; tRC=tRASmax; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N	1,200	mA	
Operating current - burst read; Burst length = 2; reads; continuous burst; One bank active; address and control inputs changing once per clock cycle; 50% of data changing at every burst; Iout = 0 mA	IDD4R	2,080	mA	
Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	IDD4W	2,360	mA	
Auto refresh current; tRC = tRFC(min), 10*tCK for DDR500 at 250MHz; distributed refresh	IDD5	2,200	mA	
Self refresh current; CKE <= 0.2V; External clock should be on;	IDD6	48	mA	
Operating current - Four bank operation; Four bank interleaving with BL=4 -Refer to the following page for detailed test condition	IDD7	3400	mA	

Note: 1. Module I_{DD} was calculated on the basis of component I_{DD} and can be differently measured according to DQ loading capacitor.

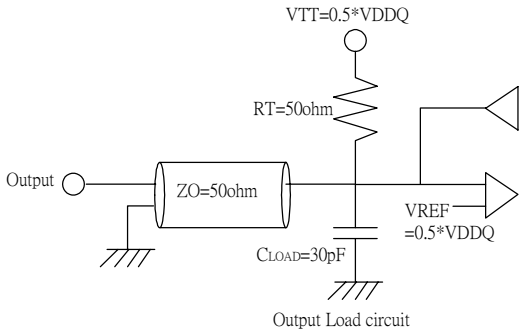
AC OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)		VREF - 0.31	V	
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ + 0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ - 0.2	0.5*VDDQ + 0.2	V	2

1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS (V_{DD}=2.6, V_{DDQ}=2.6, T_A=0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5*VDDQ	V	
Input signal maximum peak swing	1.5	V	
Input Levels (VIH/VIL)	VREF+0.31/VREF-0.31	V	
Input timing measurement reference level	VREF	V	
Output timing measurement reference level	VTT	V	
Output load condition	See Load Circuit		



Output Load circuit

INPUT / OUTPUT CAPACITANCE (V_{DD} = 2.6V, V_{DDQ} = 2.6V, T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min		
Input capacitance (A0~A12, BA0~BA1, /RAS, /CAS, /WE)	C_{IN1}	65	81	pF
Input capacitance (CKE0)	C_{IN2}	42	50	pF
Input capacitance (/CS0)	C_{IN3}	42	50	pF
Input capacitance (CK0~CK2)	C_{IN4}	28	34	pF
Input capacitance (DM0~DM7)	C_{IN5}	10	12	pF
Data and DQS input/output capacitance (DQ0~DQ63)	C_{OUT1}	10	12	pF

AC TIMING PARAMETERS & SPECIFICATIONS

(These AC characteristics were tested on the Component)

Parameter	Symbol	Min	Max	Unit	Note
Row cycle time	tRC	55		ns	
Refresh row cycle time	tRFC	70		ns	
Row active time	tRAS	40	70K	ns	
/RAS to /CAS delay	tRCD	15		ns	
Row active to Row active delay	tRP	15		ns	
Row active to Row active delay	tRRD	10		ns	
Write recovery time	tWR	15		ns	
Last data in to Read command	tWTR	2		tCK	
Clock cycle time	tCK	4	10	ns	16
Clock high level width	tCH	0.45	0.55	tCK	
Clock low level width	tCL	0.45	0.55	tCK	
DQS-out access time from CK /CK	tDQSCK	-0.55	0.55	ns	
Output data access time from CK /CK	tAC	-0.65	0.65	ns	
Data strobe edge to output data edge	tDQSQ		0.4	ns	13
Read Preamble	tRPRE	0.9	1.1	tCK	
Read Postamble	tRPST	0.4	0.6	tCK	
CK to valid DQS-in	tDQSS	0.72	1.28	tCK	
Write preamble setup time	tWPRES	0		ps	5
Write preamble	tWPRE	0.25		tCK	
Write postamble	tWPST	0.4	0.6	tCK	4
DQS falling edge to CK rising-setup time	tDSS	0.2		tCK	
DQS falling edge from CK rising-hold time	tDSH	0.2		tCK	
DQS-in high level width	tDQSH	0.35		tCK	
DQS-in low level width	tDQSL	0.35		tCK	
Address and Control input setup time	tIS	0.6		ns	7~10
Address and Control input hold time	tIH	0.6		ns	7~10
Data-out high-impedance time from CK, /CK	tHZ	-	tAC max	ns	3
Data-out low-impedance time from CK, /CK	tLZ	tAC min	tAC max	ns	3
Mode register set cycle time	tMRD	2		ns	
DQ & DM setup time to DQS	tDS	0.4		ns	
DQ & DM hold time to DQS	tDH	0.4		ns	
DQ & DM input pulse width	tDIPW	1.75		ns	9

Control &Address input pulse width for each input	tIPW	2.2		ns	9
Refresh interval time	tREF	7.8		us	6
Output DQS valid window	TQH	tHP-tQHS		ns	12
Clock half period	tHP	tCLmin/tCHmin		ns	11,12
Data hold skew factor	tQHS		0.5	ns	12
Auto Precharge write recovery + precharge time	tDAL	-	-	ns	14
Exit self refresh to non-read command	tXSNR	75		ns	
Exit self refresh to read command	tXSRD	200		ns	

Note:
1. VID is the magnitude of the difference between the input level on CK and the input level on CK.
2. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.
3. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output in no longer driving (HZ), or begins driving (LZ).
4. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but sys tem performance (bus turnaround) will degrade accordingly.
5. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
6. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
7. For command/address input slew rate $\geq$ 0.5 V/ns
8. For CK & CK slew rate $\geq$ 0.5 V/ns
9. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
10. Slew Rate is measured between VOH(ac) and VOL(ac).
11. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH)..... For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into
12. tQH = tHP - tQHS, where: tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
13. tDQSQ:Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
14. tDAL = (tWR/tCK) + (tRP/tCK)
15. In all circumstances, tXSNR can be satisfied using tXSNR=tRFCmin+1*tCK
16. The only time that the clock frequency is allowed to change is during self-refresh mode.

SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	$BA_{0,1}$	A_{10}/AP	A_0~A_9, A_{11}, A_{12}	Note
Register	Extended Mode Register Set		H	X	L	L	L	L	OP CODE			1,2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down	Entry		H	L	H	X	X	X	X			
					L	V	V	V				
	Exit		L	H	X	X	X	X				
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X			
					L	H	H	H				
	Exit		L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X			8
No Operation Command			H	X	H	X	X	X	X			9
					L	H	H	H				9

Note:
1. OP Code: Operand Code. A0 ~ A12 & BA0 ~ BA1: Program keys. (@EMRS/MRS)
2. EMRS/ MRS can be issued only at all banks precharge state. A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM. The automatically precharge without row precharge command is meant by "Auto". Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1: Bank select addresses. If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected. If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected. If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected. If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command cannot be issued. Another bank read/write command can be issued after the end of burst. New row active of the associated bank can be issued at tRP after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in is masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation (NOP)" in DDR SDRAM.

SERIAL PRESENCE DETECT SPECIFICATION

Serial Presence Detect			
Byte No.	Function Described	Standard Specification	Vendor Part
0	# of Bytes Written into Serial Memory	128bytes	80
1	Total # of Bytes of S.P.D Memory	256bytes	08
2	Fundamental Memory Type	DDR SDRAM	07
3	# of Row Addresses on this Assembly	13	0D
4	# of Column Addresses on this Assembly	10	0A
5	# of Module Rows on this Assembly	2 bank	02
6	Data Width of this Assembly	64bits	40
7	Data Width of this Assembly	0	00
8	VDDQ and Interface Standard of this Assembly	SSTL-2	04
9	DDR SDRAM Cycle Time at CAS Latency=3	4ns	40
10	DDR SDRAM Access Time from Clock at CL=3	±0.65ns	65
11	DIMM configuration type (non-parity, Parity, ECC)	Non ECC	00
12	Refresh Rate Type	7.8us/Self Refresh	82
13	Primary DDR SDRAM Width	X8	08
14	Error Checking DDR SDRAM Width	X0	00
15	Min Clock Delay for Back to Back Random Column Address	tCCD=1CLK	01
16	Burst Lengths Supported	2,4,8	0E
17	# of banks on each DDR SDRAM device	4 bank	04
18	CAS Latency supported	3	10
19	CS Latency	0 CLK	01
20	WE Latency	1 CLK	02
21	DDR SDRAM Module Attributes	Differential Clock Input	20
22	DDR SDRAM Device Attributes: General	-	00
23	DDR SDRAM Cycle Time CL=2.5	-	00
24	DDR SDRAM Access from Clock CL=2.5	-	00
25	DDR SDRAM Cycle Time CL=2.0	-	0
26	DDR SDRAM Access from Clock CL=2.0	-	0
27	Minimum Row Precharge Time (tRP)	15ns	3C
28	Minimum Row Active to Row Activate delay (tRRD)	10ns	28
29	Minimum RAS to CAS Delay (tRCD)	15ns	3C
30	Minimum active to Precharge time (tRAS)	40ns	28
31	Module ROW density	256MB	40
32	Command/Address Input Setup Time	0.6ns	60
33	Command/Address Input Hold Time	0.6ns	60
34	Data Signal Input Setup Time	0.4ns	40
35	Data Signal Input Hold Time	0.4ns	40
36-40	Superset Information	-	00
41	DDR SDRAM Minimum Active to Active/Auto Refresh Time(tRC)	-	00
42	DDR SDRAM Minimum Auto-Refresh to	-	00

	Active/Auto-Refresh Command Period (tRFC)		
43	DDR SDRAM Maximum Device Cycle Time (tCK max)	-	00
44	DDR SDRAM DQS-DQ Skew for DQS and associated DQ signals (tDQSQ max)	-	00
45	DDR SDRAM Read Data Hold Skew Factor (tQHS)	-	00
46	PLL Relock Time	-	00
47~61	Superset Information	-	00
62	SPD Data Revision Code	REV 1.0	00
63	Checksum for Bytes 0-62	A9	A9
64-71	Manufacturers JEDEC ID	Transcend	7F, 4F
72	Manufacturing Location	T	54
73-90	Manufacturers Part Number	TS64MLD64V5F	54 53 36 34 4D 4C 44 36 34 56 35 46 20 20 20 20 20 20
91-92	Revision Code	-	-
93-94	Manufacturing Date	By Manufacturer	Variable
95-98	Assembly Serial Number	By Manufacturer	Variable
99-127	Manufacturer Specific Data	-	-
128~255	Unused Storage Locations	Undefined	-